TPS82130 具有集成电感的 17V 输入、3A 降压转换器 MicroSiP™模块

1 特性

- 3.0mm x 2.8mm x 1.5mm MicroSiP™封装
- 输入电压范围：3.0V 至 17V
- 3A 持续输出电流
- DCS-Control™拓扑技术
- 在轻负载条件下实现高效率的省电模式
- 20µA 静态工作电流
- 0.9V 至 6V 可调节输出电压
- 可实现最低压降的 100% 占空比
- 电源正常输出
- 具有跟踪功能的可编程软启动
- 热关断保护
- -40°C 至 125°C 的工作温度范围
- 借助 WEBENCH® 电源设计器，使用 TPS82130 创建定制设计方案

2 应用

- 工业 应用
- 电信和网络 应用
- 固态硬盘

3 说明

TPS82130 是一款 17V 输入、3A 降压转换器 MicroSiP™电源模块，经优化兼具小型解决方案尺寸和高效率优势。该模块集成了同步降压转换器和电感，可简化设计、减少外部元件数量并节省印刷电路板 (PCB) 的面积。该器件采用紧凑的薄型封装，适合通过标准表面贴装设备自动组装。

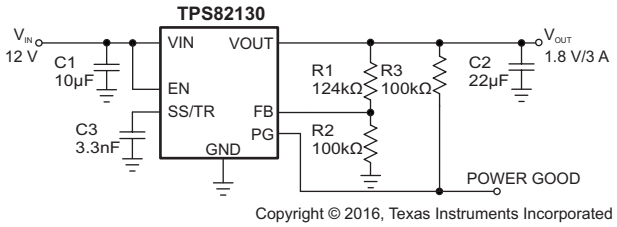
为了最大限度地提升效率，此转换器以 2MHz 的标称开关频率在 PWM 模式下工作，并在轻负载电流下自动进入省电运行模式。在节能模式下，该器件静态工作电流的典型值为 20µA。凭借 DCS-Control™拓扑，器件可获得出色的负载瞬态性能和精确的输出稳压。

器件信息(1)

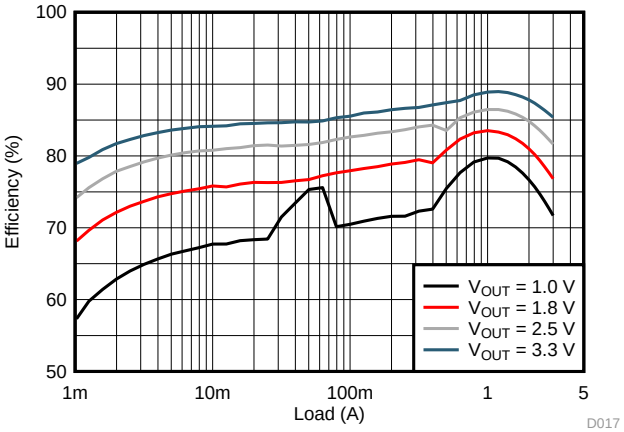
器件型号	封装	封装尺寸（标称值）
TPS82130SIL	µSiL (8)	3.0mm x 2.8mm x 1.5mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化原理图
1.8V 输出应用



12V 输入电压效率



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (August 2016) to Revision C **Page**

- 已添加 WEBENCH 信息至*特性*、*详细设计流程*和*器件支持*部分 1
- Changed the Output voltage MAX value From: 5 V to: 6 V in the *Recommend Operating Conditions* table 4
- 已添加 表 1, Power Good Pin Logic 10

Changes from Revision A (February 2015) to Revision B **Page**

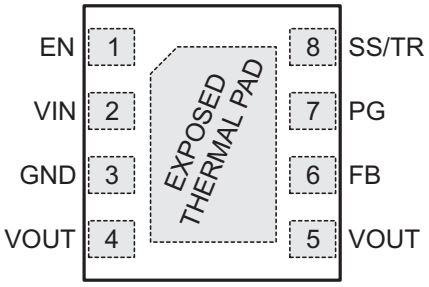
- Changed storage temperature to -55°C from -40°C 4
- Updated thermal information 4
- Added FB voltage accuracy at T_J = 0°C to 85°C condition 5
- 已更改 derating curve based on ambient temperature 13
- 已更改 derating curve based on ambient temperature 13
- 已添加 derating curve for V_{OUT} = 1.0 V 14
- 已删除 Thermal pictures 17
- 已添加 增加了“接收文档更新通知”部分。 18

Changes from Original (December 2015) to Revision A **Page**

- 量产数据发布 1

5 Pin Configuration and Functions

8-Pin μSiL Package
(SIL0008C Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable pin. Pull High to enable the device. Pull Low to disable the device. This pin has an internal pull-down resistor of typically 400kΩ when the device is disabled.
VIN	2	PWR	Input pin.
GND	3		Ground pin.
VOUT	4,5	PWR	Output pin.
FB	6	I	Feedback reference pin. An external resistor divider connected to this pin programs the output voltage.
PG	7	O	Power good open drain output pin. A pull-up resistor can be connected to any voltage less than 6V. Leave it open if it is not used.
SS/TR	8	I	Soft startup and voltage tracking pin. An external capacitor connected to this pin sets the internal reference voltage rising time.
Exposed Thermal Pad			The exposed thermal pad must be connected to the GND pin. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Voltage at pins(2)	VIN	-0.3	20	V
	EN, SS/TR	-0.3	V_{IN} + 0.3	
	PG, FB	-0.3	7	
	VOUT	0	7	
Sink current	PG		10	mA
Module operating temperature		–40	125	°C
Storage temperature		–55	125	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommend Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
V_{IN}	Input voltage	3	17	V
V_{PG}	Power good pull-up resistor voltage		6	V
V_{OUT}	Output voltage	0.9	6	V
I_{OUT}	Output current	0	3	A
T_J	Module operating temperature range for 100,000 hours lifetime(1)	-40	110	°C

(1) The module operating temperature range includes module self temperature rise and IC junction temperature rise. In applications where high power dissipation is present, the maximum operating temperature or maximum output current must be derated. For applications where the module operates continuously at 125 °C temperature, the maximum lifetime is reduced to 50,000 hours.

6.4 Thermal Information

THERMAL METRIC(1)		TPS82130 (JEDEC 51-5)	TPS82130EVM-720	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.2	46.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.4	9.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	14.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.2	14.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	21.3	21.3	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953. Theta-JA can be improved with a custom PCB design containing thermal vias where possible.

6.5 Electrical Characteristics

T_J = -40°C to 125°C and V_{IN} = 3.0V to 17V. Typical values are at T_J = 25°C and V_{IN} = 12V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
I_Q	Quiescent current into VIN	No load, device not switching			20	35	µA
I_{SD}	Shutdown current into VIN	EN = Low			1.5	7.4	µA
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling		2.6	2.7	2.8	V
		V_{IN} rising		2.8	2.9	3.0	V
T_{JSD}	Thermal shutdown threshold	T_J rising			160		°C
		T_J falling			140		°C
LOGIC INTERFACE (EN)							
V_{IH}	High-level input voltage			0.9	0.65		V
V_{IL}	Low-level input voltage				0.45	0.3	V
$I_{lkg(EN)}$	Input leakage current into EN pin	EN = High			0.01	1	µA
CONTROL (SS/TR, PG)							
$I_{SS/TR}$	SS/TR pin source current			2.1	2.5	2.8	µA
V_{PG}	Power good threshold	V_{OUT} rising, referenced to V_{OUT} nominal		92%	95%	99%	
		V_{OUT} falling, referenced to V_{OUT} nominal		87%	90%	94%	
$V_{PG,OL}$	Power good low-level voltage	I_{sink} = 2mA			0.1	0.3	V
$I_{lkg(PG)}$	Input leakage current into PG pin	V_{PG} = 1.8V			1	400	nA
OUTPUT							
V_{FB}	Feedback regulation voltage	PWM mode		785	800	815	mV
			T_J = 0°C to 85°C	788	800	812	
		PSM	C_{OUT} = 22 µF	785	800	823	
			C_{OUT} = 2x22 µF, T_J = 0°C to 85°C	788	800	815	
$I_{lkg(FB)}$	Feedback input leakage current	V_{FB} = 0.8V			1	100	nA
	Line regulation	I_{OUT} = 1A, V_{OUT} = 1.8V			0.002		%/V
	Load regulation	I_{OUT} = 0.5A to 3A, V_{OUT} = 1.8V			0.12		%/A
POWER SWITCH							
$R_{DS(on)}$	High-side FET on-resistance	I_{SW} = 500mA, V_{IN} ≥ 6V			90	170	mΩ
		I_{SW} = 500mA, V_{IN} = 3V			120		
	Low-side FET on-resistance	I_{SW} = 500mA, V_{IN} ≥ 6V			40	70	
		I_{SW} = 500mA, V_{IN} = 3V			50		
R_{DP}	Dropout resistance	100% mode, V_{IN} ≥ 6V			125		mΩ
		100% mode, V_{IN} = 3V			160		
I_{LIMF}	High-side FET switch current limit	V_{IN} = 6V, T_A = 25°C		3.6	4.2	4.9	A
f_{SW}	PWM switching frequency	I_{OUT} = 1A, V_{OUT} = 1.8V			2.0		MHz

6.6 Typical Characteristics

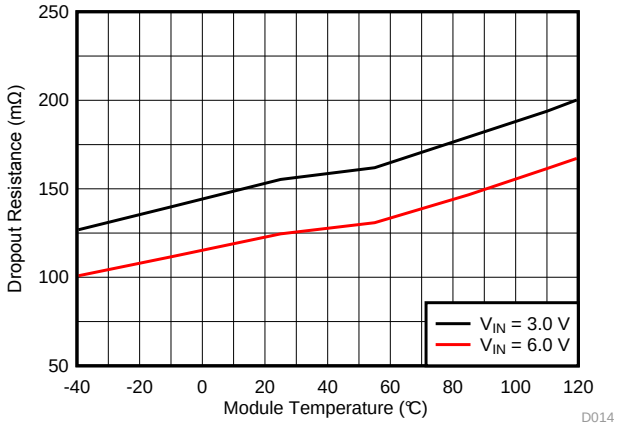


图 1. Dropout Resistance

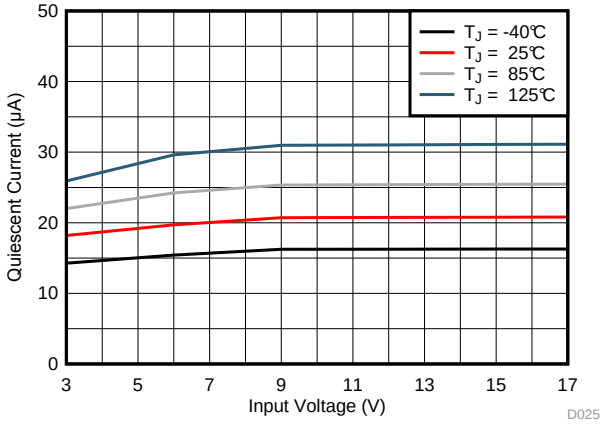


图 2. Quiescent Current

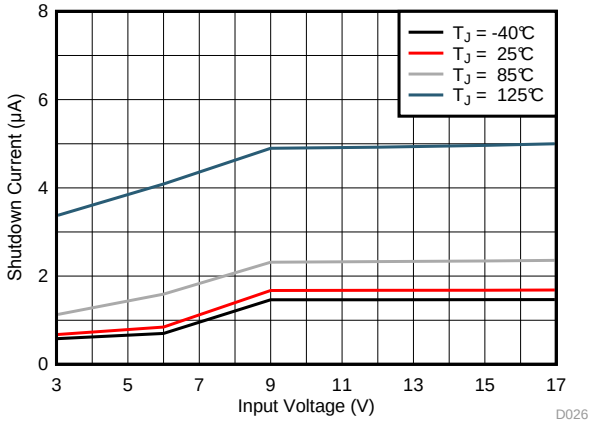


图 3. Shutdown Current

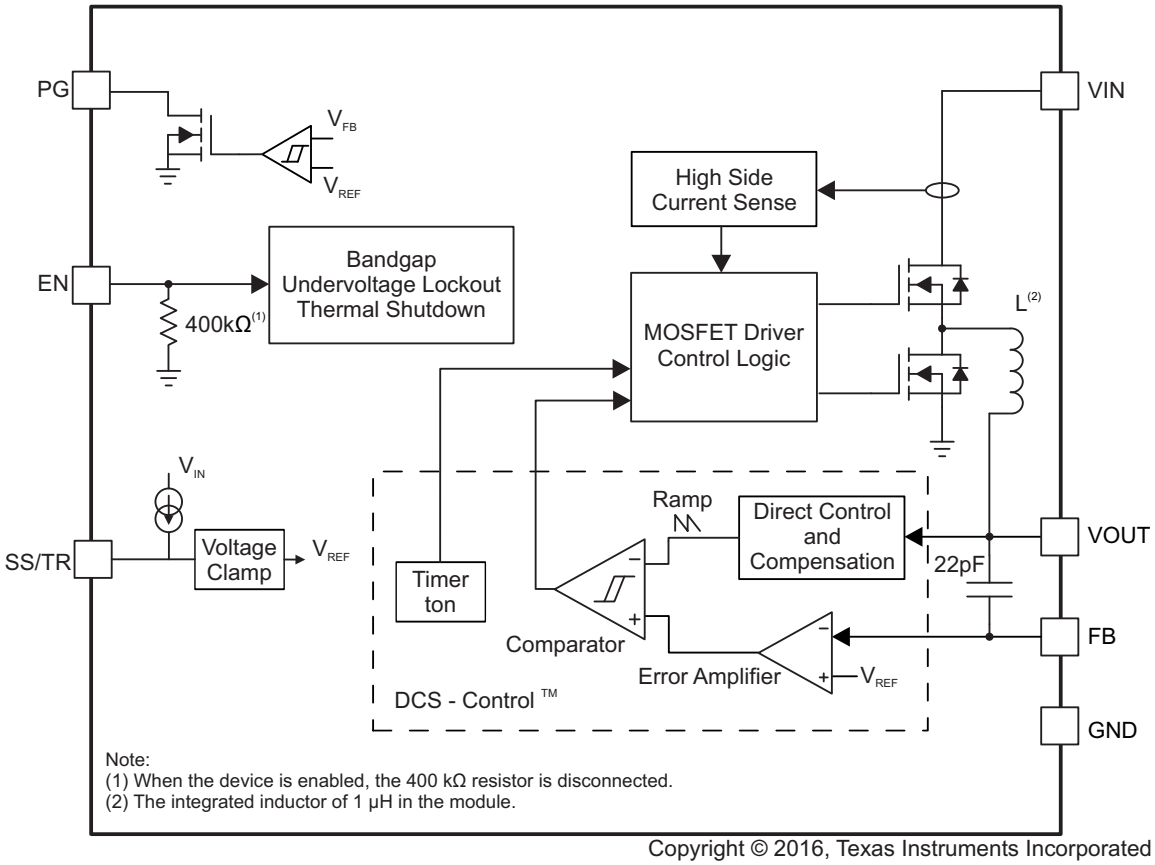
7 Detailed Description

7.1 Overview

The TPS82130 synchronous step-down converter MicroSiP™ power module is based on DCS-Control™ (Direct Control with Seamless transition into Power Save Mode). This is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control.

The DCS-Control™ topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in PSM (Power Save Mode) at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 2.0MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC's quiescent current to achieve high efficiency over the entire load current range. DCS-Control™ supports both operation modes using a single building block and therefore has a seamless transition from PWM to PSM without effects on the output voltage. The TPS82130 offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM and PSM Operation

The TPS82130 includes an on-time (t_{ON}) circuitry. This t_{ON}, in steady-state operation in PWM and PSM modes, is estimated as:

$$t_{ON} = 500ns \times \frac{V_{OUT}}{V_{IN}} \quad (1)$$

Feature Description (接下页)

In PWM mode, the TPS82130 operates with pulse width modulation in continuous conduction mode (CCM) with a t_{ON} shown in 公式 1 at medium and heavy load currents. A PWM switching frequency of typically 2.0MHz is achieved by this t_{ON} circuitry. The device operates in PWM mode as long as the output current is higher than half the inductor's ripple current estimated by 公式 2.

$$\Delta I_L = t_{ON} \times \frac{V_{IN} - V_{OUT}}{L} \quad (2)$$

To maintain high efficiency at light loads, the device enters Power Save Mode seamlessly when the load current decreases. This happens when the load current becomes smaller than half the inductor's ripple current. In PSM, the converter operates with reduced switching frequency and with a minimum quiescent current to maintain high efficiency. PSM is also based on the t_{ON} circuitry. The switching frequency in PSM is estimated as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \quad (3)$$

In PSM, the output voltage rises slightly above the nominal output voltage in PWM mode. This effect is reduced by increasing the output capacitance. The output voltage accuracy in PSM operation is reflected in the electrical specification table and given for a 22-µF output capacitor.

For very small output voltages, an absolute minimum on-time of about 80ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Also the off-time can reach its minimum value at high duty cycles. The output voltage remains regulated in such cases.

When V_{IN} decreases to typically 15% above V_{OUT}, the TPS82130 can't enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

7.3.2 Low Dropout Operation (100% Duty Cycle)

The TPS82130 offers a low input to output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} \times R_{DP} \quad (4)$$

Where

R_{DP} = Resistance from V_{IN} to V_{OUT}, including high-side FET on-resistance and DC resistance of the inductor

$V_{OUT(min)}$ = Minimum output voltage the load can accept.

7.3.3 Switch Current Limit

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a heavy load/shorted output circuit condition. If the inductor peak current reaches the switch current limit after a propagation delay of typically 30 ns, the high-side FET is turned off and the low-side FET is turned on to ramp down the inductor current.

7.3.4 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, an under voltage lockout is implemented, which shuts down the devices at voltages lower than V_{UVLO} with a hysteresis of 200 mV.

7.3.5 Thermal Shutdown

The device goes into thermal shutdown and stops switching once the junction temperature exceeds T_{JSD}. Once the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic High. Accordingly, the shutdown mode is forced if the EN pin is pulled Low with a shutdown current of typically 1.5 μA.

An internal pull-down resistor of 400kΩ is connected to the EN pin when the EN pin is Low. The pull-down resistor is disconnected when the EN pin is High.

7.4.2 Soft Startup (SS/TR)

The internal voltage clamp controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. When the EN pin is pulled high, the device starts switching after a delay of typically 55μs and the output voltage rises with a slope controlled by an external capacitor connected to the SS/TR pin. Using a very small capacitor or leaving the SS/TR pin floating provides fastest startup time.

The TPS82130 is able to start into a pre-biased output capacitor. During the pre-biased startup, both the power MOSFETs are not allowed to turn on until the internal voltage clamp sets an output voltage above the pre-bias voltage.

When the device is in shutdown, undervoltage lockout or thermal shutdown, the capacitor connected to SS/TR pin is discharged by an internal resistor. Returning from those states causes a new startup sequence.

7.4.3 Voltage Tracking (SS/TR)

The SS/TR pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in 图 4.

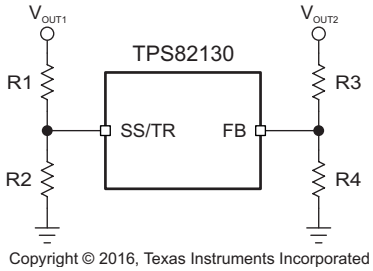


图 4. Output Voltage Tracking

When the SS/TR pin voltage is between 50 mV and 1.2 V, the VOUT2 tracks the VOUT1 as described in 公式 5.

$$\frac{V_{OUT2}}{V_{OUT1}} \approx 0.64 \times \frac{R2}{R1+R2} \times \frac{R3+R4}{R4} \quad (5)$$

When the SS/TR pin voltage is above 1.2 V, the voltage tracking is disabled and the FB pin voltage is regulated at 0.8 V. For decreasing SS/TR pin voltage, the device doesn't sink current from the output. So the resulting decreases of the output voltage may be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is VIN+0.3V.

Details about tracking and sequencing circuits are found in SLVA470.

Device Functional Modes (接下页)

7.4.4 Power Good Output (PG)

The device has a power good (PG) output. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open drain output and is specified to sink up to 2 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 6 V.

The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin floating when it is not used. 表 1 shows the PG pin logic.

表 1. Power Good Pin Logic

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	$V_{FB} \geq V_{TH\_PG}$	√	
	$V_{FB} \leq V_{TH\_PG}$		√
Shutdown (EN=Low)			√
UVLO	$0.7\ V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} < 0.7\ V$	√	

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The output voltage of the TPS82130 is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Applications

8.2.1 1.8-V Output Application

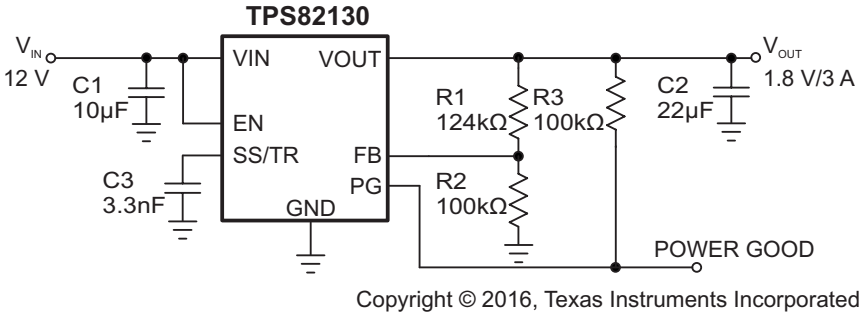


图 5. 1.8-V Output Application

8.2.1.1 Design Requirements

For this design example, use the following as the input parameters.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12V
Output voltage	1.8V
Output ripple voltage	< 20mV
Output current rating	3A

The components used for measurements are given in the following table.

表 3. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 µF, 25 V, X7R, ±20%, size 1206, C3216X7R1E106M160AE	TDK
C2	22 µF, 10 V, ±20%, X7S, size 0805, C2012X7S1A226M125AC	TDK
C3	3300 pF, 50 V, ±5%, C0G/NP0, size 0603, GRM1885C1H332JA01D	Murata
R1, R2, R3	Standard	

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TLV62090 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   – Run electrical simulations to see important waveforms and circuit performance
   – Run thermal simulations to understand the thermal performance of your board
   – Export your customized schematic and layout into popular CAD formats
   – Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Setting the Output Voltage

The output voltage is set by an external resistor divider according to the following equations:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \quad (6)$$

R2 should not be higher than 100kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. Larger currents through R2 improve noise sensitivity and output voltage accuracy. 图 5 shows the external resistor divider value for a 1.8-V output. Choose appropriate resistor values for other outputs.

In case the FB pin gets opened, the device clamps the output voltage at the VOUT pin internally to about 7V.

8.2.1.2.3 Input and Output Capacitor Selection

For best output and input voltage filtering, low ESR ceramic capacitors are required. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. A 10-µF or larger input capacitor is required. The output capacitor value can range from 22µF up to more than 400µF. Higher values are possible as well and can be evaluated through the transient response. Larger soft start times are recommended for higher output capacitances.

High capacitance ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

8.2.1.2.4 Soft Startup Capacitor Selection

A capacitance connected between the SS/TR pin and the GND allows programming the startup slope of the output voltage. A constant current of 2.5 µA charges the external capacitor. The capacitance required for a given soft startup time for the output voltage is given by:

$$C_{SS/TR} = t_{SS/TR} \times \frac{I_{SS/TR}}{1.25V} \quad (7)$$

8.2.1.3 Application Performance Curves

T_A = 25°C, V_{IN} = 12 V, V_{OUT} = 1.8 V, unless otherwise noted.

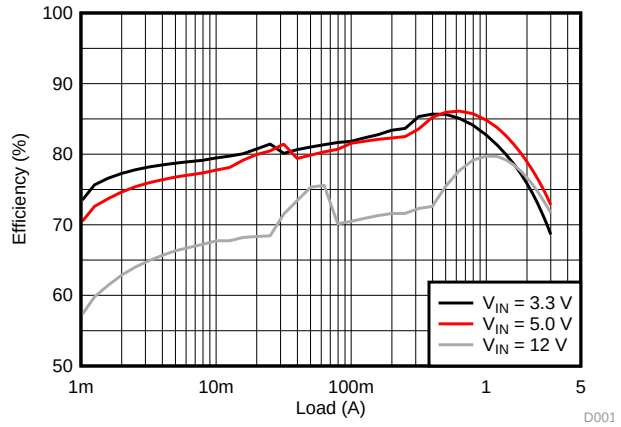


图 6. Efficiency, V_{OUT} = 1.0 V

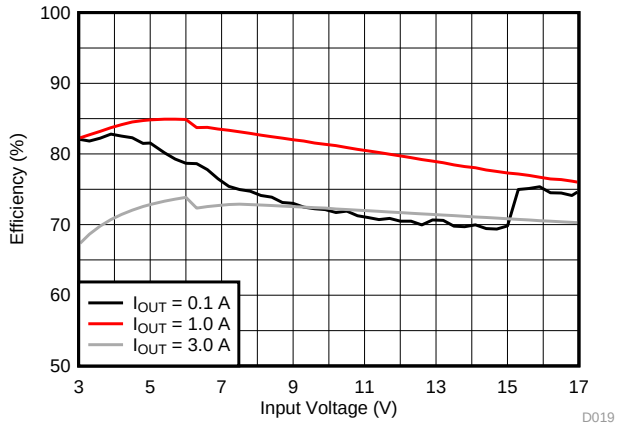


图 7. Efficiency, V_{OUT} = 1.0 V

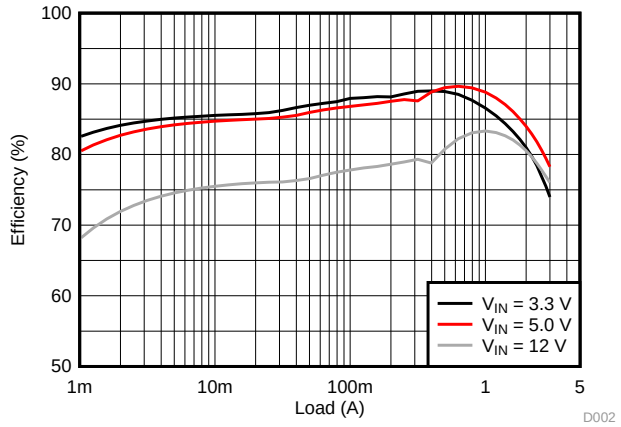


图 8. Efficiency, V_{OUT} = 1.8 V

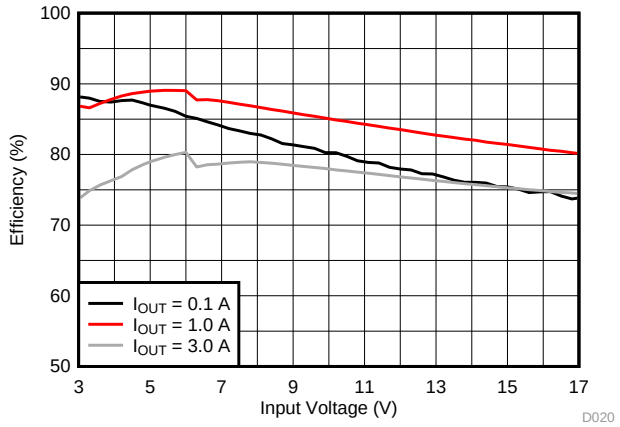


图 9. Efficiency, V_{OUT} = 1.8 V

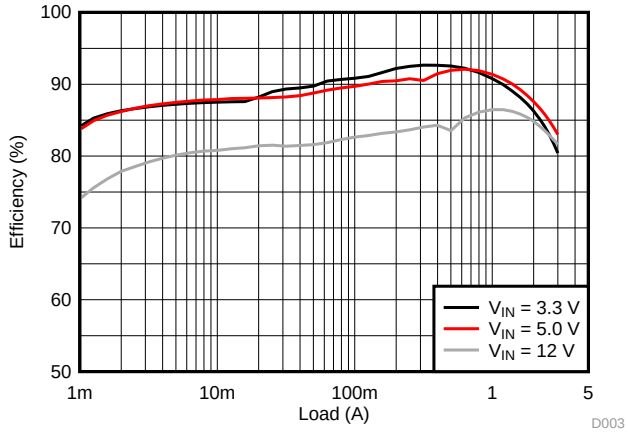


图 10. Efficiency, V_{OUT} = 2.5 V

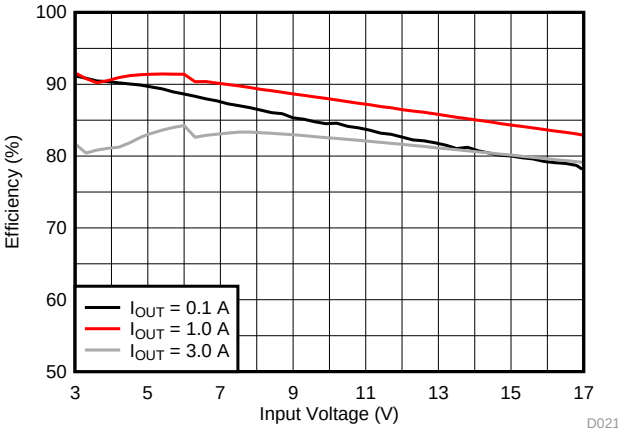


图 11. Efficiency, V_{OUT} = 2.5 V

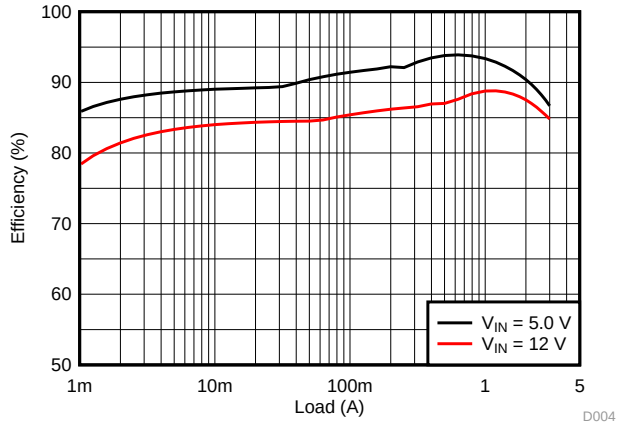


图 12. Efficiency, V_{OUT} = 3.3 V

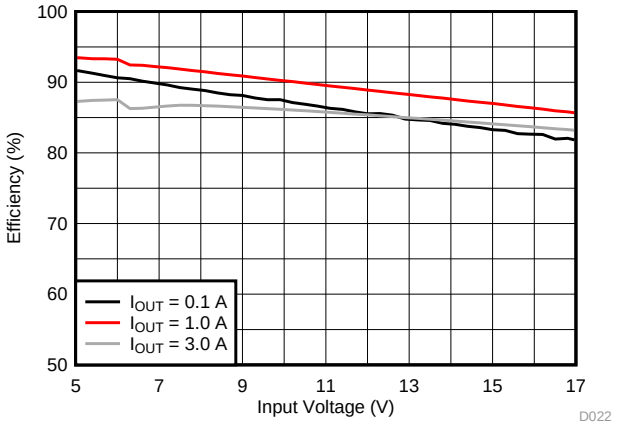


图 13. Efficiency, V_{OUT} = 3.3 V

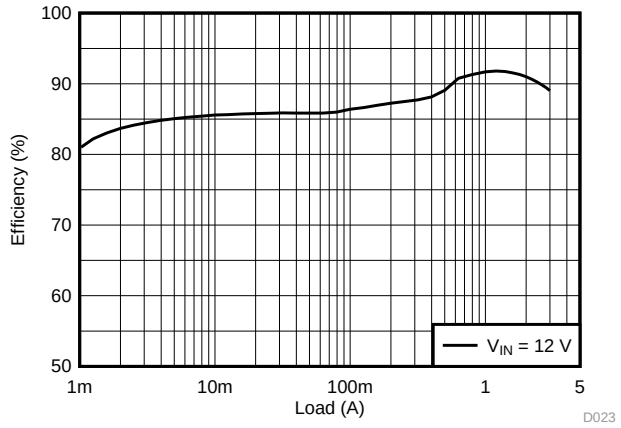


图 14. Efficiency, V_{OUT} = 5.0 V

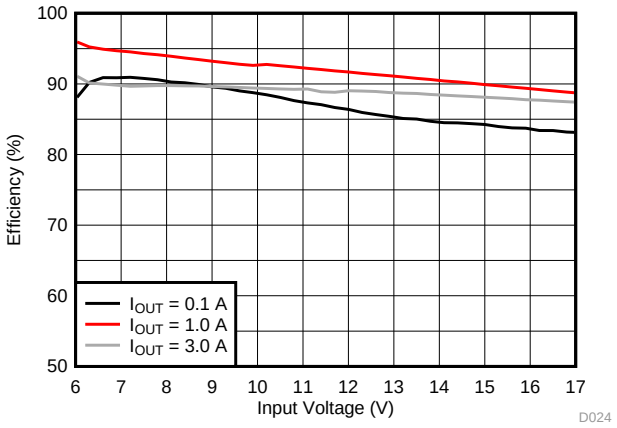
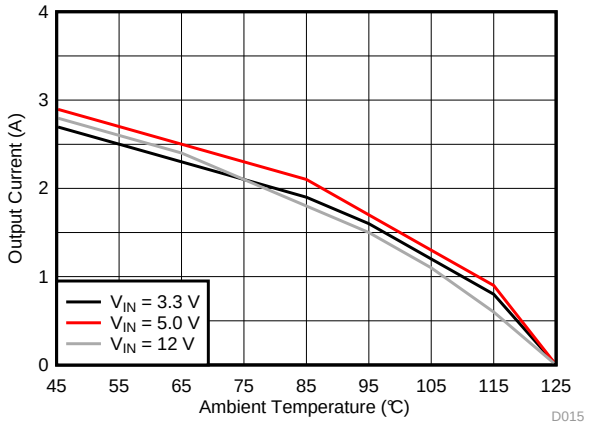
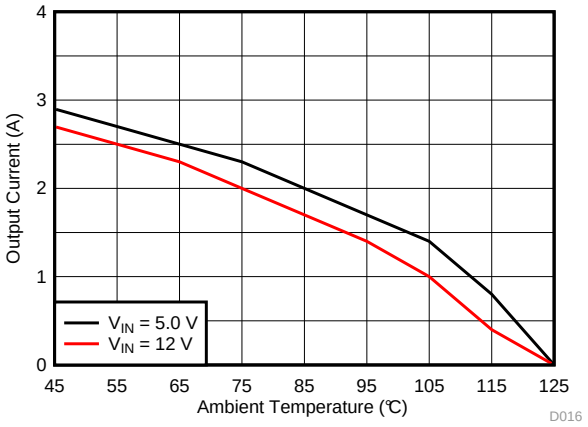


图 15. Efficiency, V_{OUT} = 5.0 V



V_{OUT} = 1.8V θ_{JA} = 46.1 °C/W

图 16. Thermal Derating, V_{OUT} = 1.8 V



V_{OUT} = 3.3V θ_{JA} = 46.1 °C/W

图 17. Thermal Derating, V_{OUT} = 3.3 V

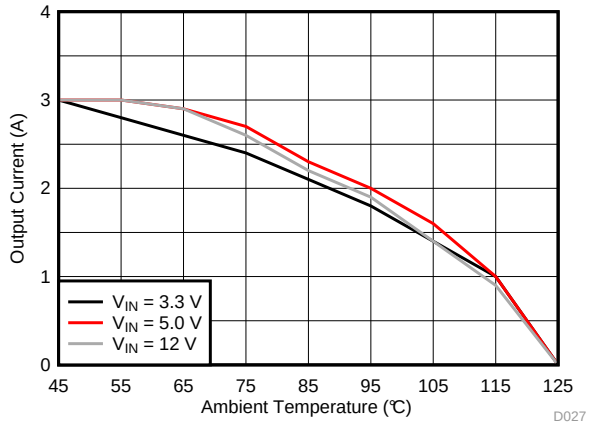
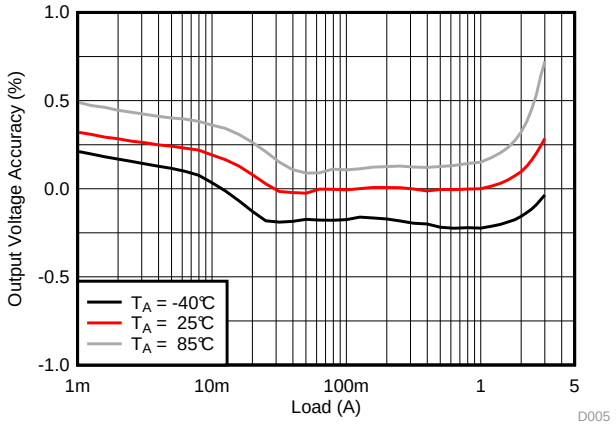
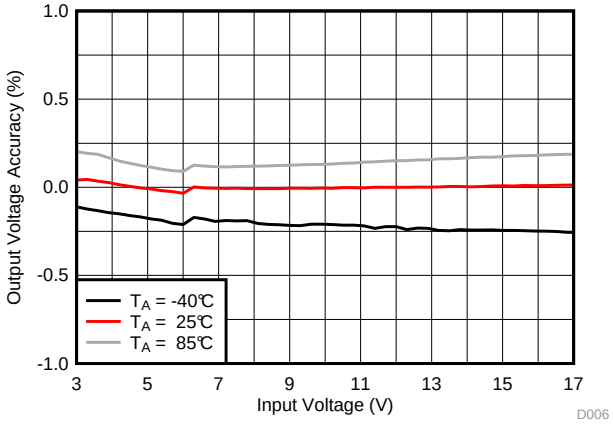


图 18. Thermal Derating, V_{OUT} = 1.0 V



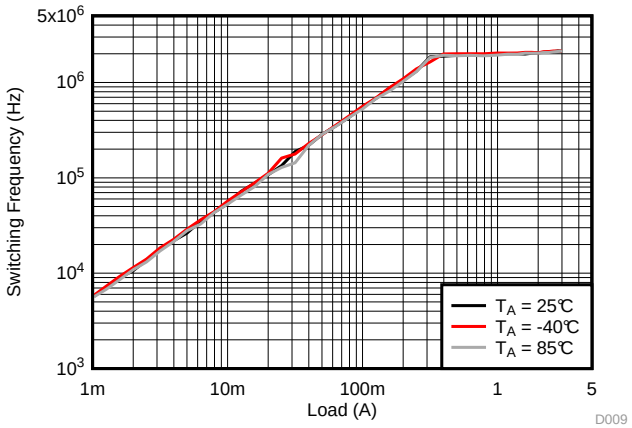
V_{IN} = 12V

图 19. Load Regulation



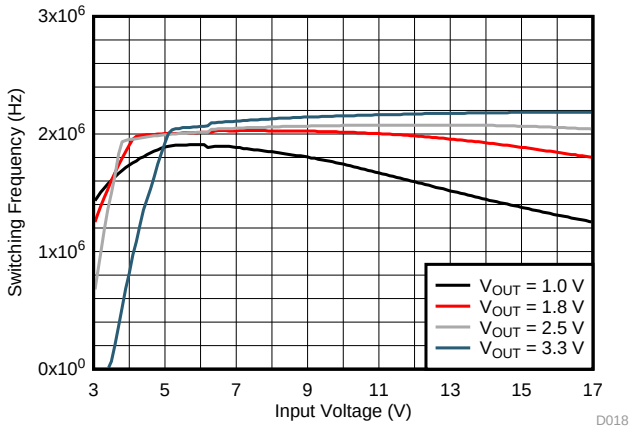
I_{OUT} = 1A

图 20. Line Regulation



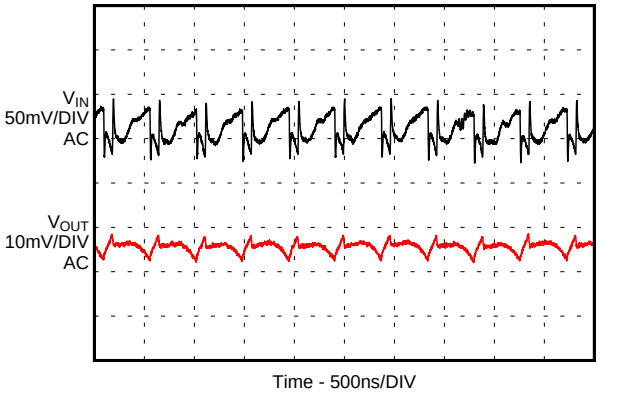
V_{OUT} = 1.8V V_{IN} = 12V

图 21. Switching Frequency



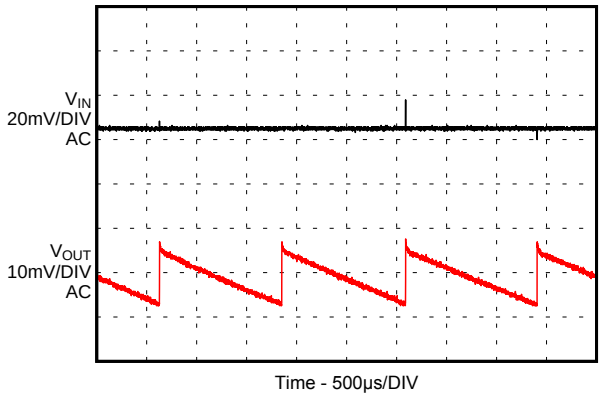
I_{OUT} = 1A

图 22. Switching Frequency



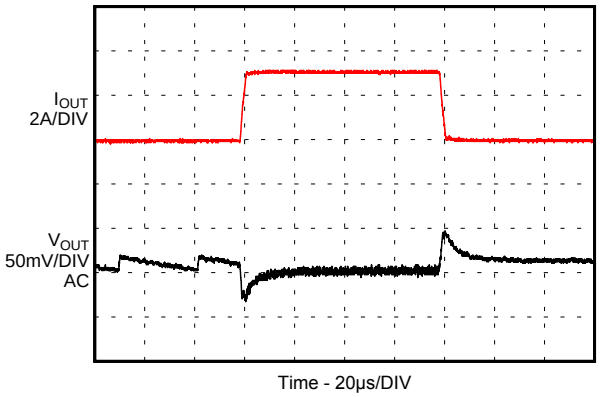
I_{OUT} = 3A

图 23. Input and Output Ripple in PWM Mode



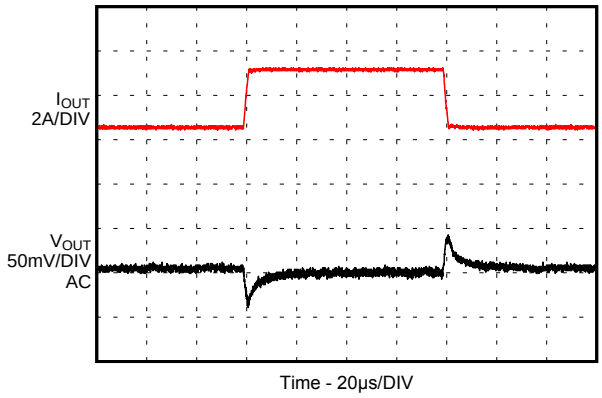
No Load

图 24. Input and Output Ripple in PSM Mode



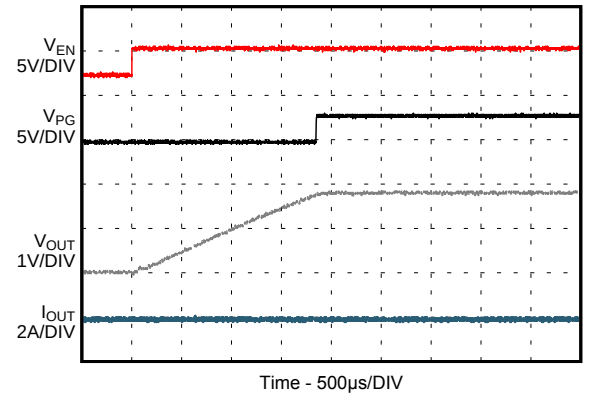
I_{OUT} = 0A to 3A, 1A/µs

图 25. Load Transient



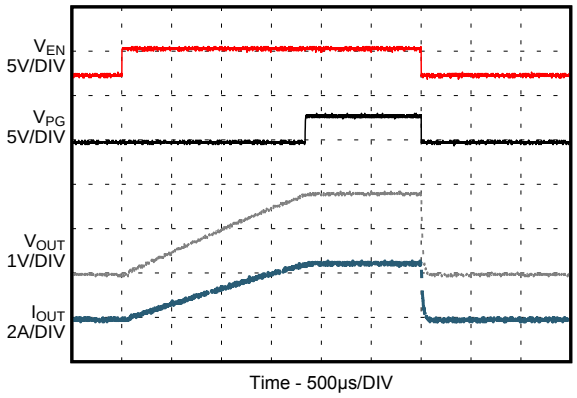
I_{OUT} = 0.5A to 3A, 1A/µs

图 26. Load Transient



No Load

图 27. Startup without Load



R_{OUT} = 0.68Ω

图 28. Startup / Shutdown with Resistance Load

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3V and 17V. The average input current of the TPS82130 is calculated as:

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \quad (8)$$

Ensure that the power supply has a sufficient current rating for the applications.

10 Layout

10.1 Layout Guidelines

- TI recommends placing all components as close as possible to the IC. The input capacitor placement specifically, must be closest to the VIN and GND pins of the device.
- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance.
- To enhance heat dissipation of the device, the exposed thermal pad should be connected to bottom or internal layer ground planes using vias.
- Refer to 图 29 for an example of component placement, routing and thermal design.

10.2 Layout Example

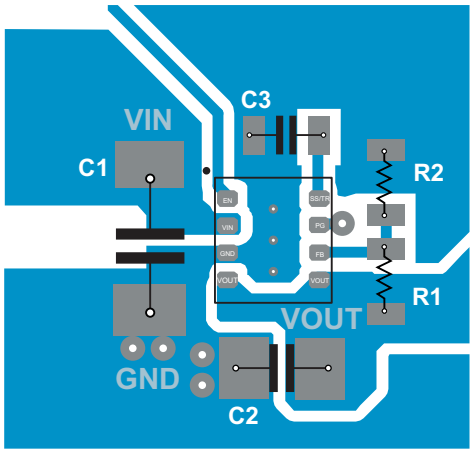


图 29. TPS82130 PCB Layout

10.3 Thermal Consideration

The output current of the TPS82130 needs to be derated when the device operates in a high ambient temperature or delivers high output power. The amount of current derating is dependent upon the input voltage, output power, PCB layout design and environmental thermal condition. Care should especially be taken in applications where the localized PCB temperature exceeds 65°C.

The TPS82130 module temperature must be kept less than the maximum rating of 125°C. Three basic approaches for enhancing thermal performance are below:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the TPS82130 to the PCB.
- Introduce airflow into the system.

To estimate approximate module temperature of TPS82130, apply the typical efficiency stated in this datasheet to the desired application condition to find the module's power dissipation. Then calculate the module temperature rise by multiplying the power dissipation by its thermal resistance. For more details on how to use the thermal parameters in real applications, see the application notes: SZZA017 and SPRA953.

11 器件和文档支持

11.1 开发支持

11.1.1 使用 WEBENCH® 工具定制设计方案

请单击此处，借助 并使用 TLV62090 器件定制设计方案 WEBENCH®Power Designer 并使用 TPS54561 器件定制设计方案。

1. 首先输入您的 V_{IN}、V_{OUT} 和 I_{OUT} 要求。
2. 使用优化器拨盘可优化效率、封装和成本等关键设计参数并将您的设计与德州仪器 (TI) 的其他可行解决方案进行比较。
3. WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。
4. 在多数情况下，您还可以：
   - 运行电气仿真，观察重要波形以及电路性能
   - 运行热性能仿真，了解电路板热性能
   - 将定制原理图和布局方案导出至常用 CAD 格式
   - 打印设计方案的 PDF 报告并与同事共享
5. 有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

11.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

MicroSiP, DCS-Control, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

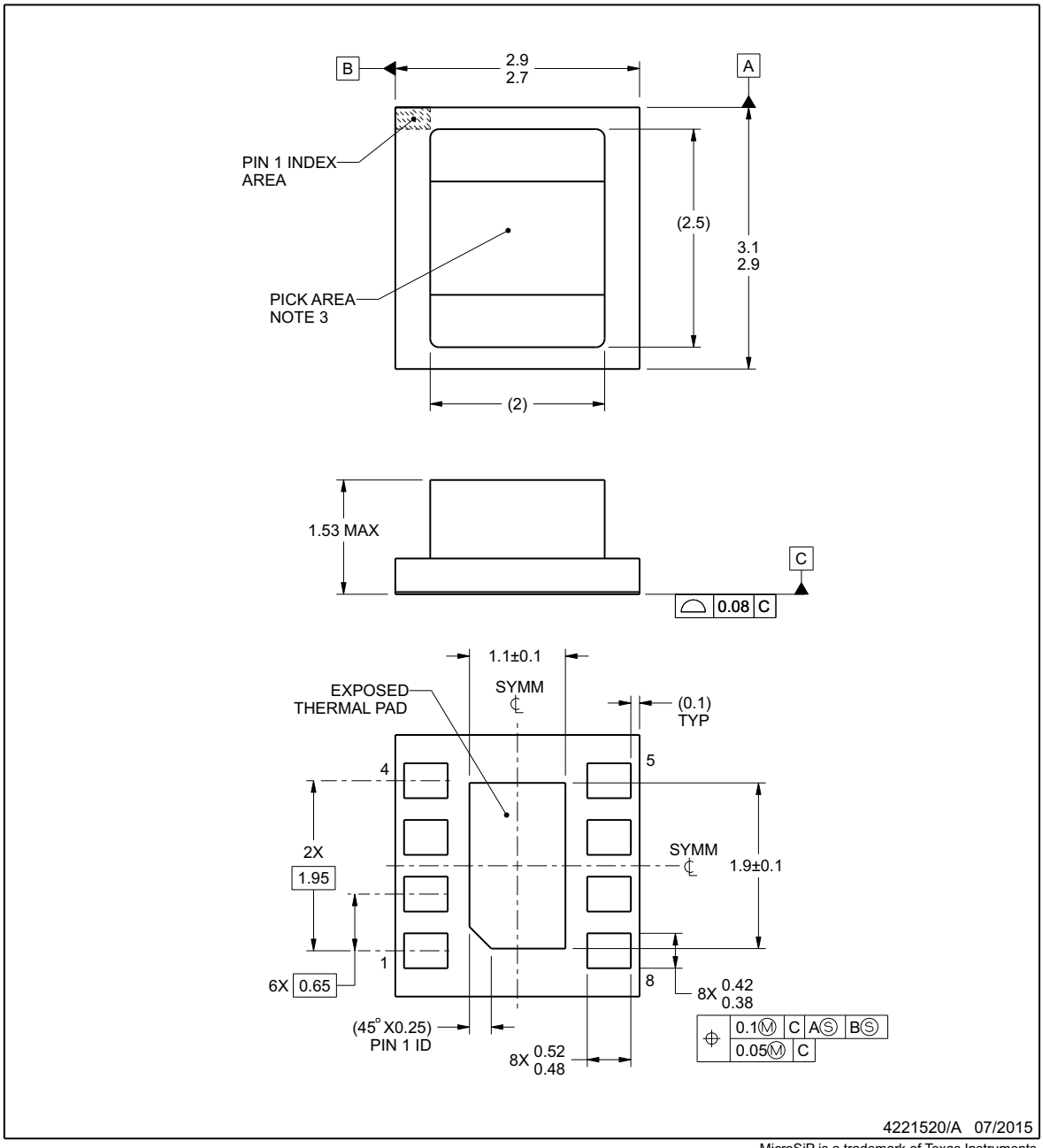
以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGE OUTLINE

SIL0008D

MicroSiP™ - 1.53 mm max height

MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments

NOTES:

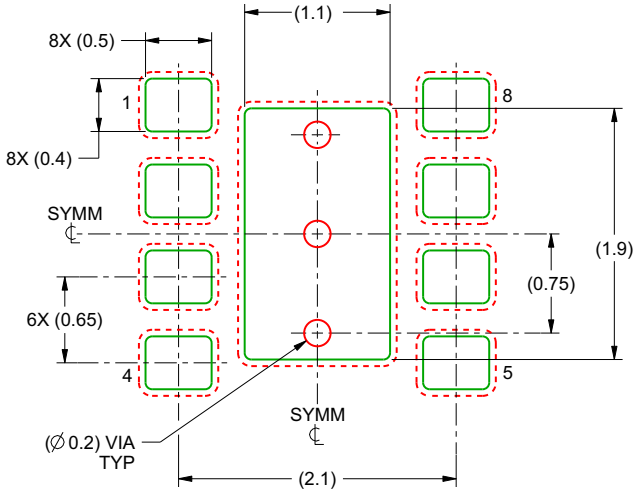
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 1.3 mm or smaller recommended.
4. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

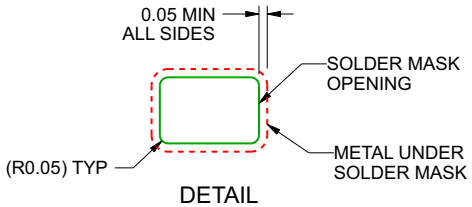
SIL0008D

MicroSiP ™ - 1.53 mm max height

MICRO SYSTEM IN PACKAGE



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:20X



DETAIL
NOT TO SCALE

4221520/A 07/2015

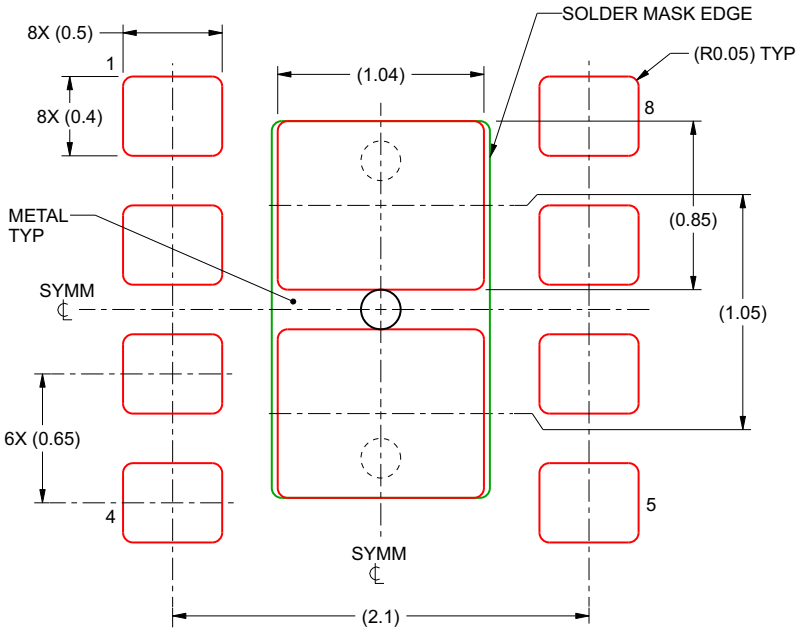
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

SIL0008D — **MicroSiP ™ - 1.53 mm max height**

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS82130SILR	ACTIVE	uSiP	SIL	8	3000	TBD	Call TI	Call TI	-40 to 125	H6 TXI1300EC	Samples
TPS82130SILT	ACTIVE	uSiP	SIL	8	250	TBD	Call TI	Call TI	-40 to 125	H6 TXI1300EC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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